

Computer Organization and Architecture

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Lecture 07



Revision

Adders

Half Adder

- Adding two single-bit binary values, X, Y produces a sum S bit and a carry out C-out bit.
- This operation is called half addition and the circuit to realize it is called a half adder.

Half Adder Truth Table

Inputs		Outputs	
X	Y	S	C-out
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



$$S(X, Y) = \Sigma (1, 2)$$

$$S = X'Y + XY'$$

$$S = X \oplus Y$$

$$C\text{-out}(x, y, C\text{-in}) = \Sigma (3)$$

$$C\text{-out} = XY$$



Full Adder

- A combinational circuit that adds 3 input bits to generate a Sum bit and a Carry bit

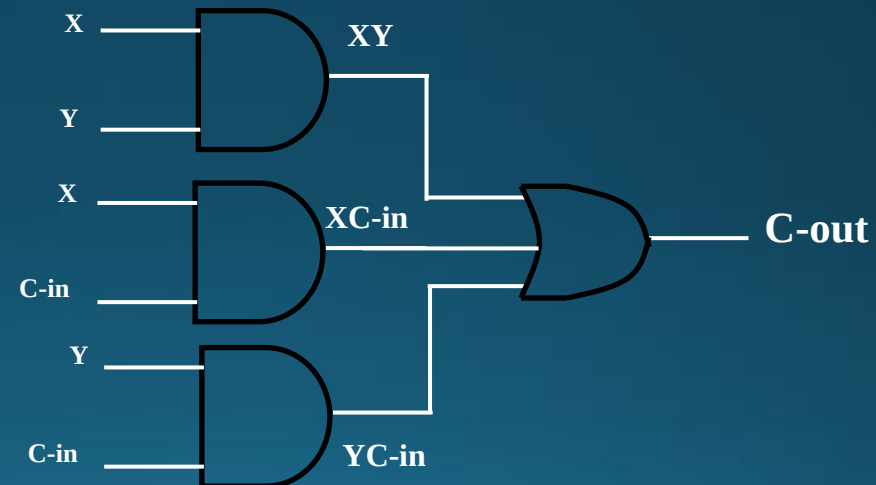
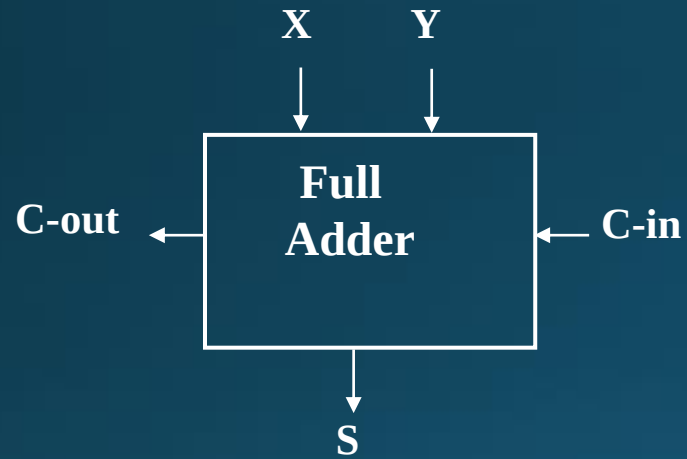
- A truth table and sum of minterm equations for C and S are shown below.

	X	Y	Z	C	S
	0	0	0	0	0
	0	0	1	0	1
	0	1	0	0	1
$0 + 1 + 1 = 10 \rightarrow$	0	1	1	1	0
	1	0	0	0	1
	1	0	1	1	0
	1	1	0	1	0
$1 + 1 + 1 = 11 \rightarrow$	1	1	1	1	1

$$C(X,Y,Z) = \sum m(3,5,6,7)$$

$$S(X,Y,Z) = \sum m(1,2,4,7)$$

Full Adder Circuit Using XOR



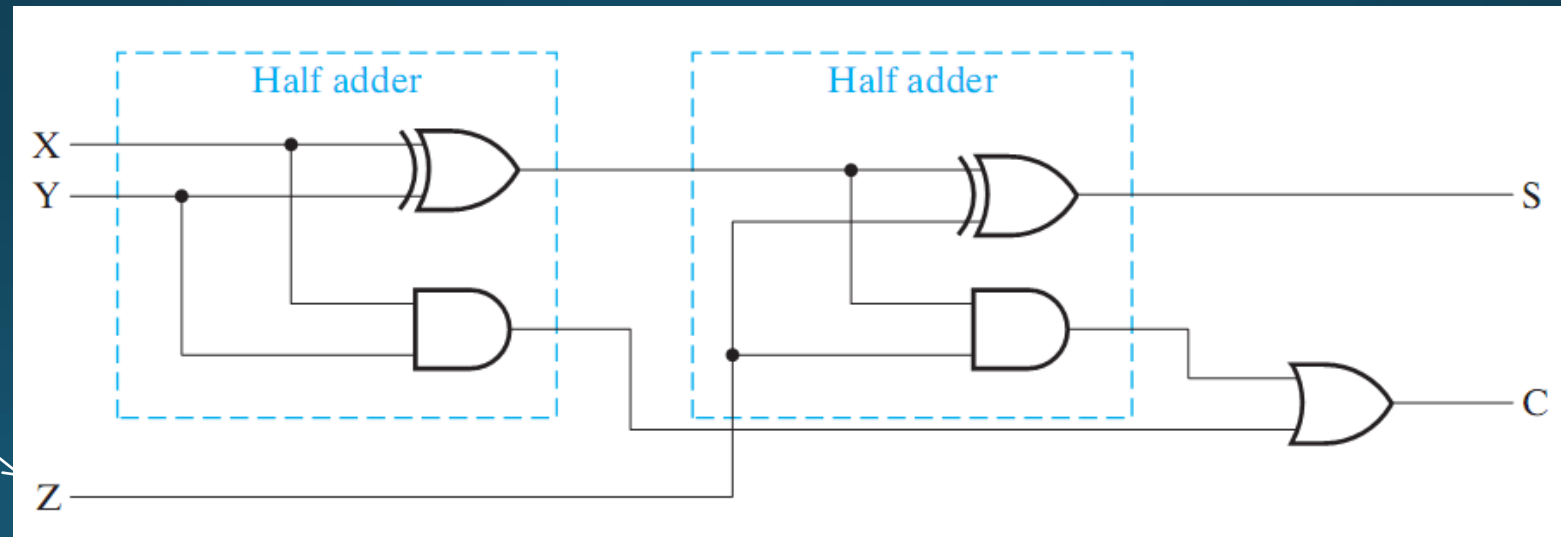
Full Adder = 2 Half Adders

Manipulating the Equations:

$$S = (X \oplus Y) \oplus Z$$

$$C = XY + XZ + YZ = XY + Z(X \oplus Y)$$

Think of
Z as a
carry in



SRC: Mano's BOOK

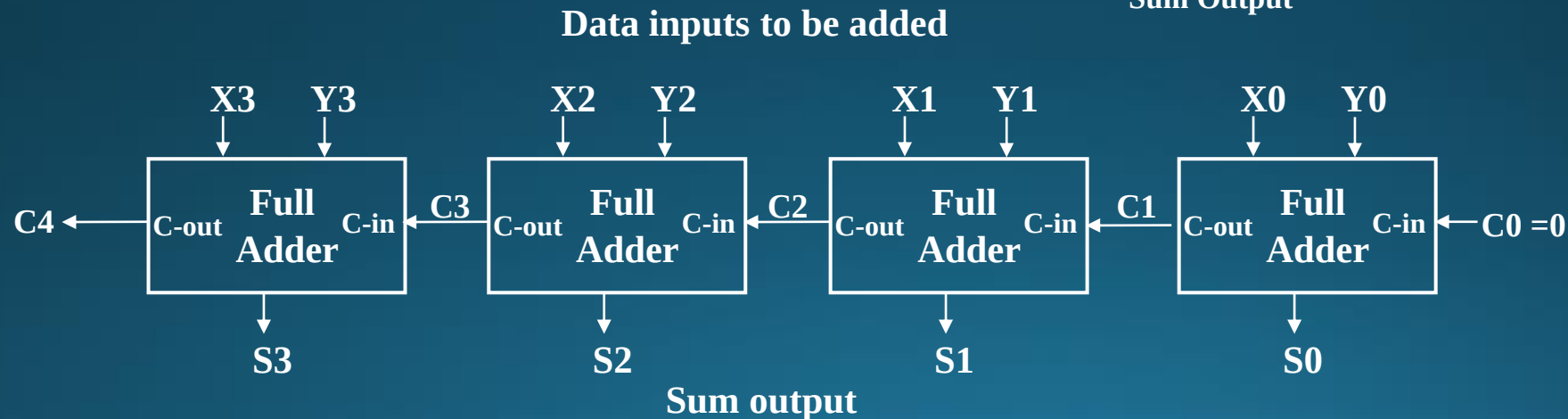
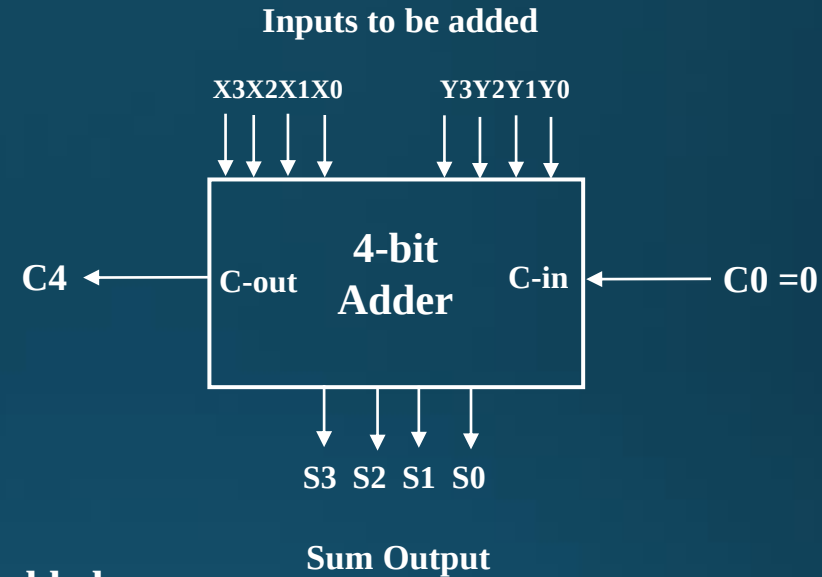
4-bit Carry Ripple Adder

Adds two 4-bit numbers:

$X = X_3 \ X_2 \ X_1 \ X_0$

$Y = Y_3 \ Y_2 \ Y_1 \ Y_0$

producing the sum $S = S_3 \ S_2 \ S_1 \ S_0$,
 $C\text{-out} = C_4$ from the most significant position $j=3$



Subtractors

Half Subtractor

- Subtracting a single-bit binary value Y from another X (I.e. $X - Y$) produces a difference bit D and a borrow out bit $B\text{-out}$.
- This operation is called half subtraction and the circuit to realize it is called a half subtractor.

Half Subtractor Truth Table

Inputs		Outputs	
X	Y	D	$B\text{-out}$
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



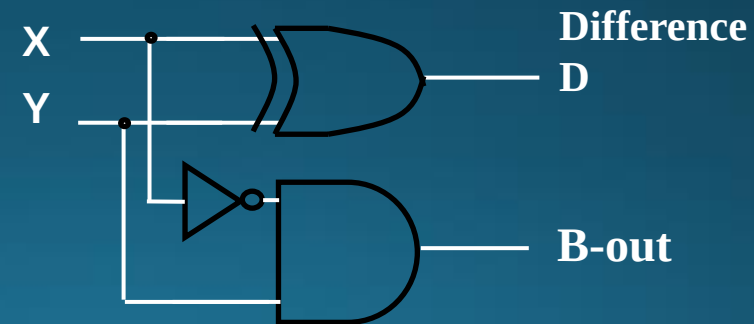
$$D(X, Y) = \Sigma (1, 2)$$

$$D = X'Y + XY'$$

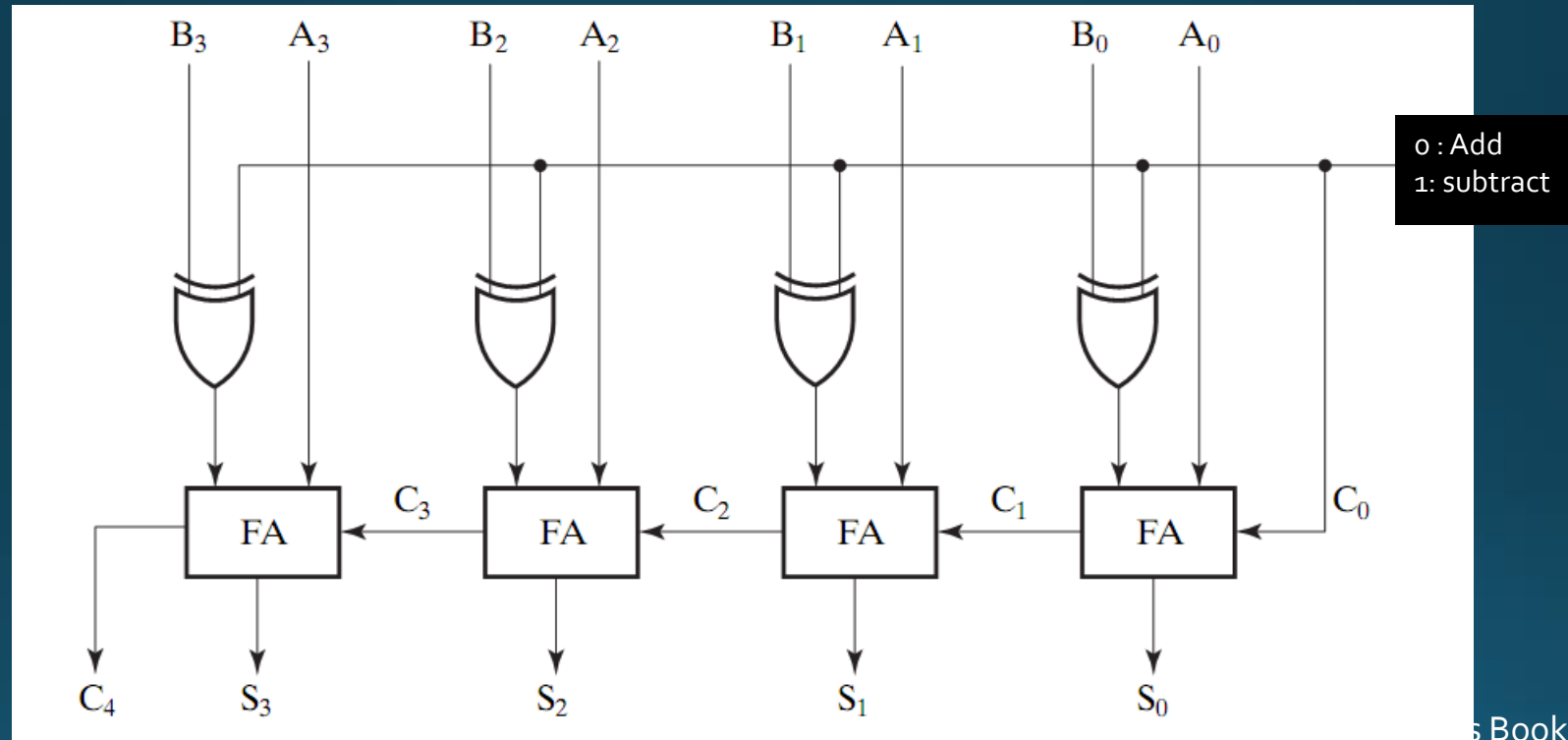
$$D = X \oplus Y$$

$$B\text{-out}(x, y, C\text{-in}) = \Sigma (1)$$

$$B\text{-out} = X'Y$$



Adder/Subtractor



Using full adders and XOR we can build an Adder/Subtractor!

Digital Circuits

Digital Circuits

- Decoders
- Encoders

Decoders

Decoder

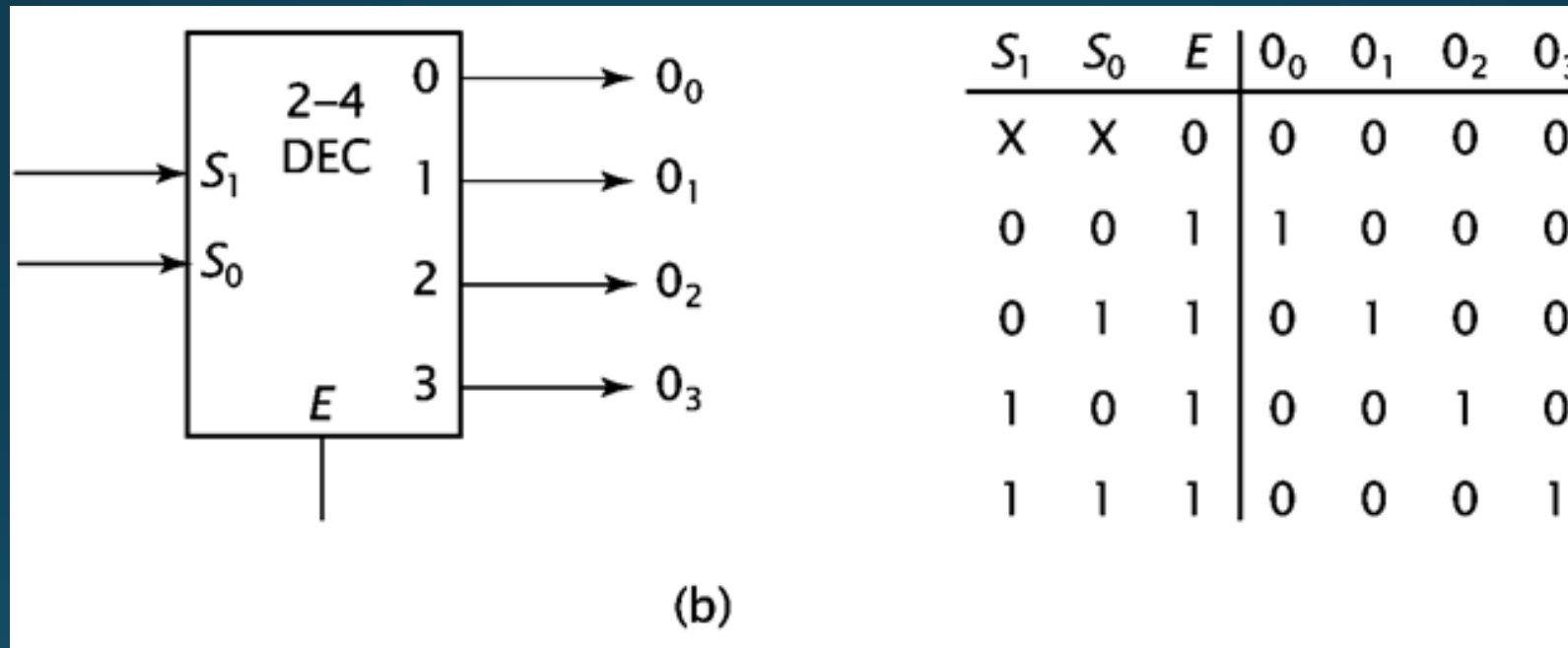
Accepts a value and decodes it

- Output corresponds to value of n inputs

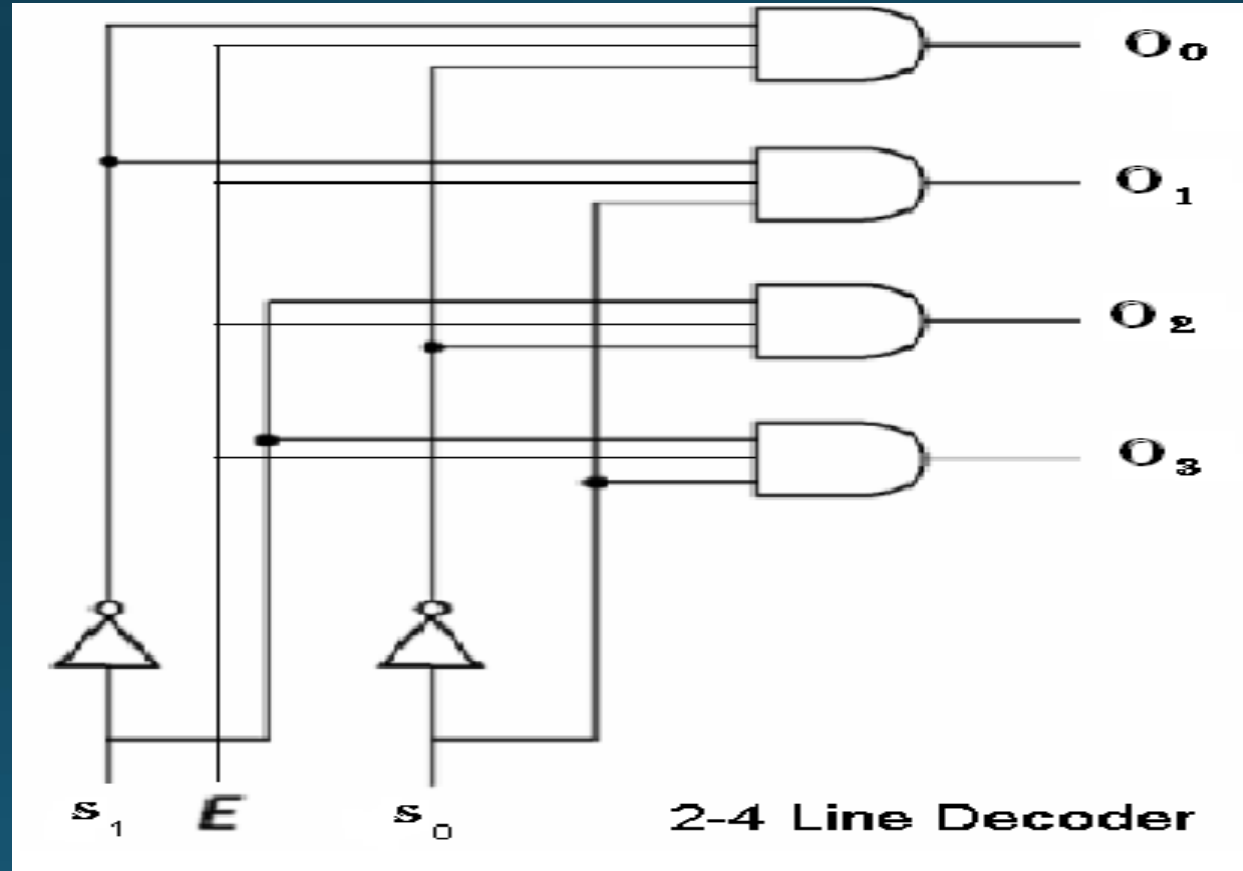
Consists of:

- Inputs (n)
- Outputs (2^n , numbered from $0 \rightarrow 2^n - 1$)
- Selectors / Enable (active high or active low)

2-to-4 Decoder



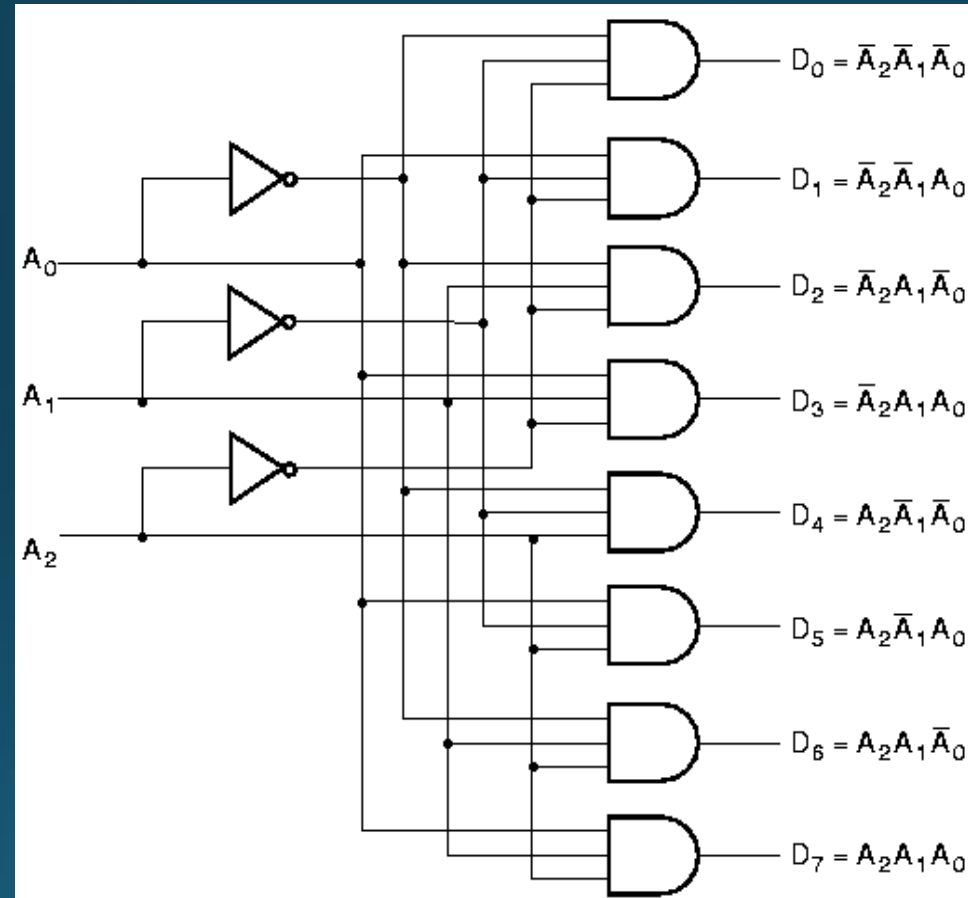
2-to-4 Decoder



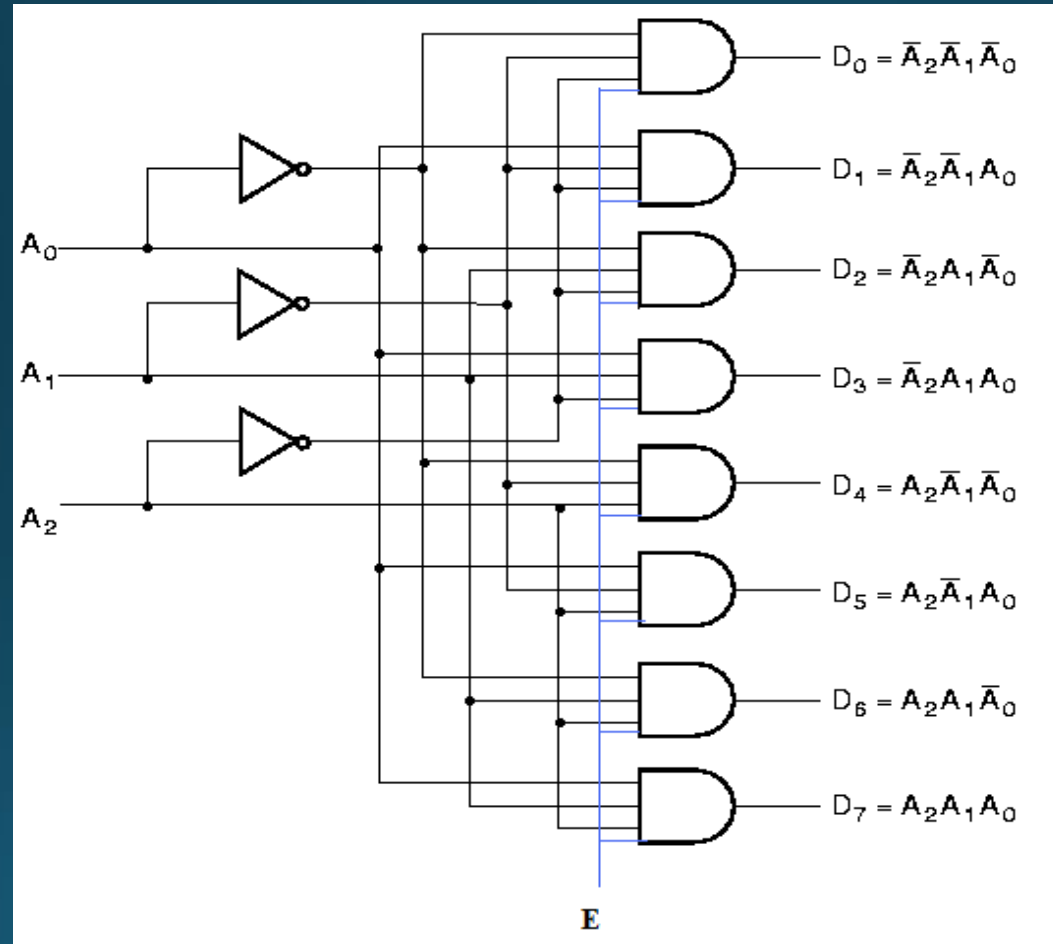
The truth table of 3-to-8 Decoder

A2	A1	A0	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

3-to-8 Decoder

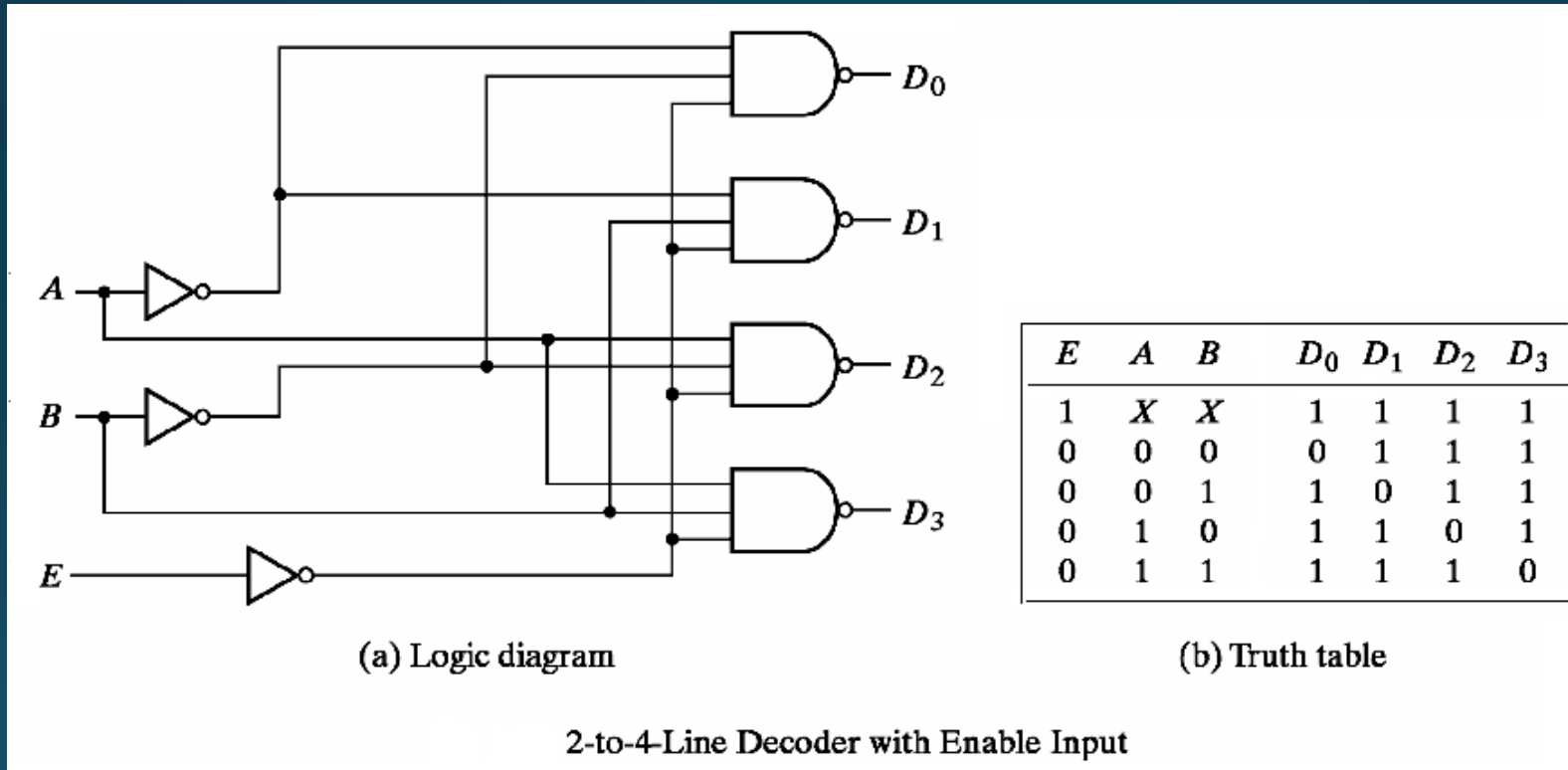


3-to-8 Decoder with Enable

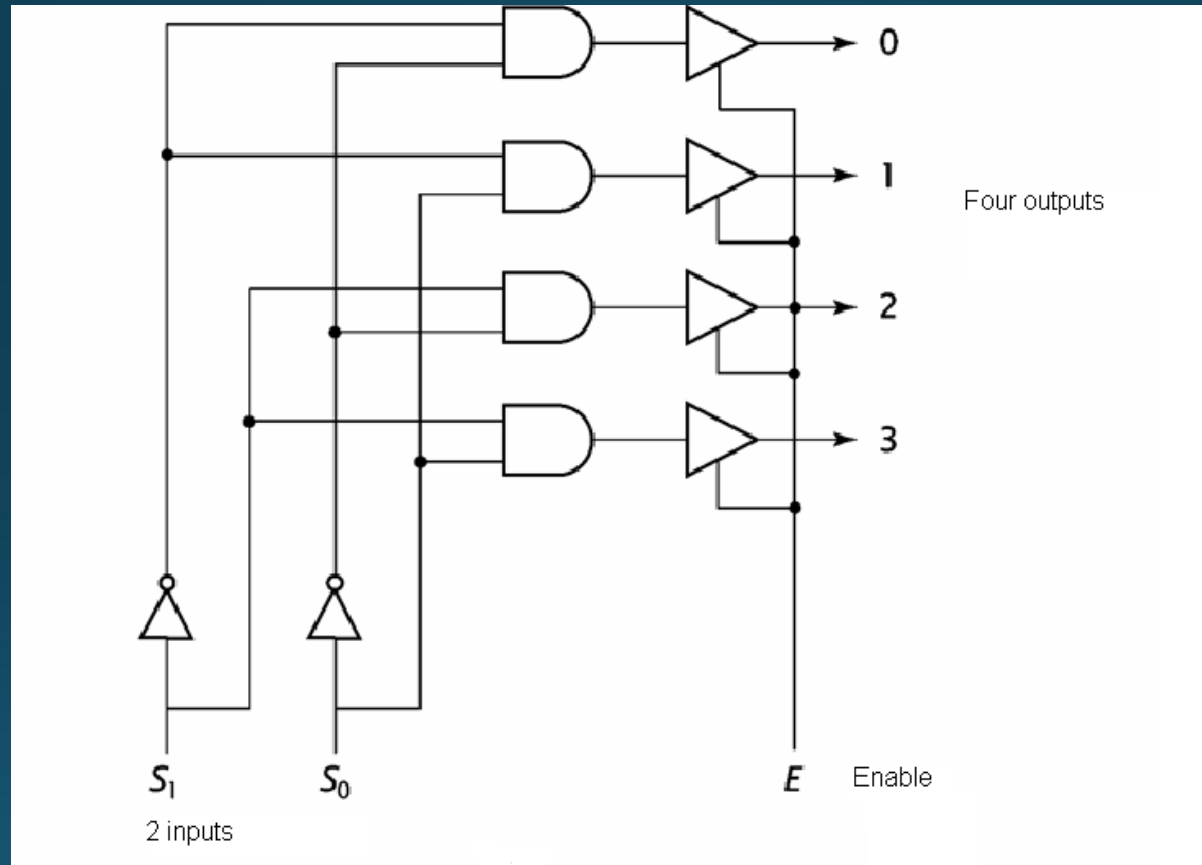


2-to-4 Decoder: NAND implementation

Decoder is enabled when $E=0$ and an output is active if it is 0



2-4 Decoder with 2-input and Enable



Decoder Expansion

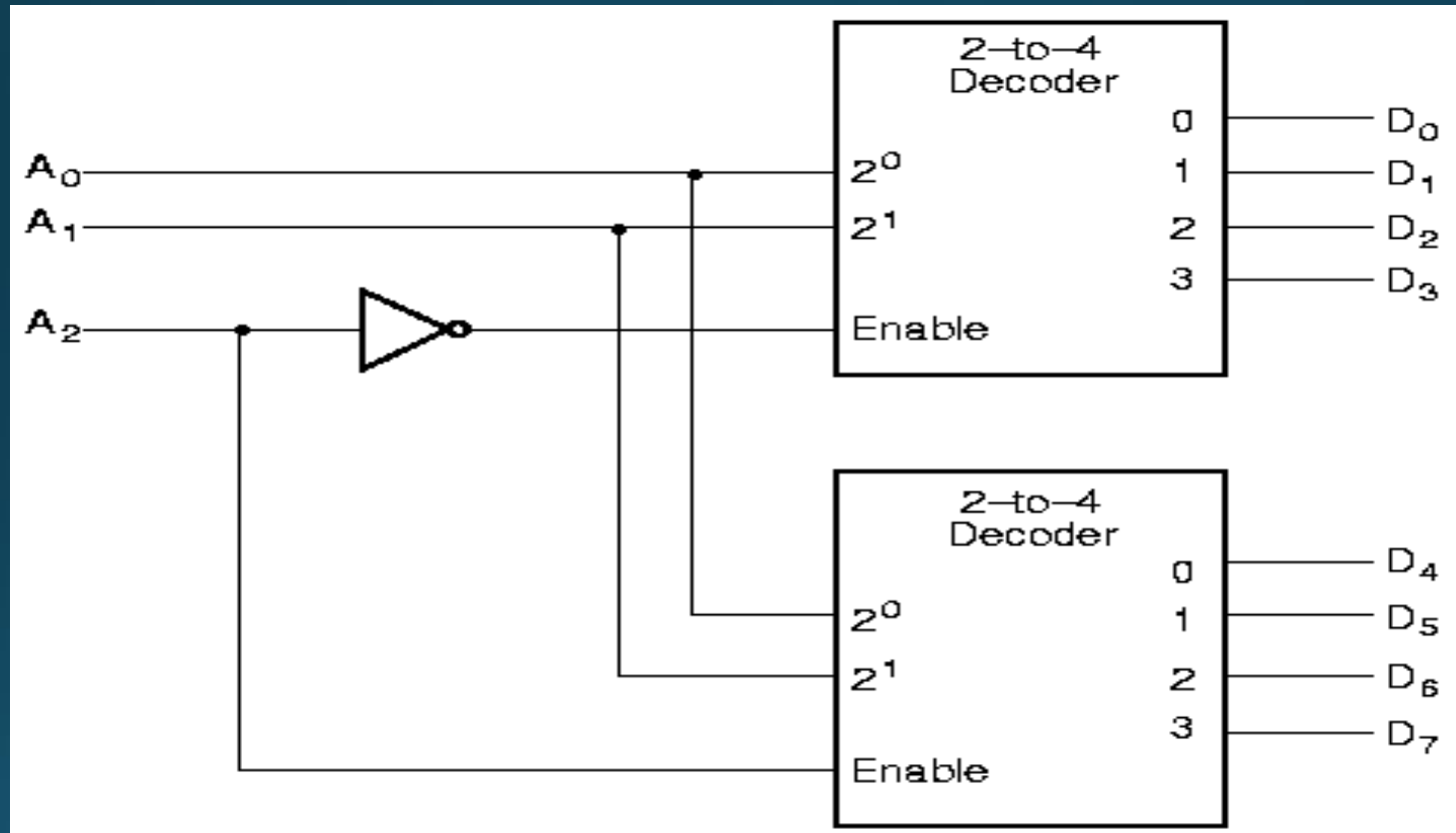
Decoder expansion

Combine two or more small decoders with enable inputs to form a larger decoder

3-to-8-line decoder constructed from two 2-to-4-line decoders

- The MSB is connected to the enable inputs
- if $A_2=0$, upper is enabled; if $A_2=1$, lower is enabled.

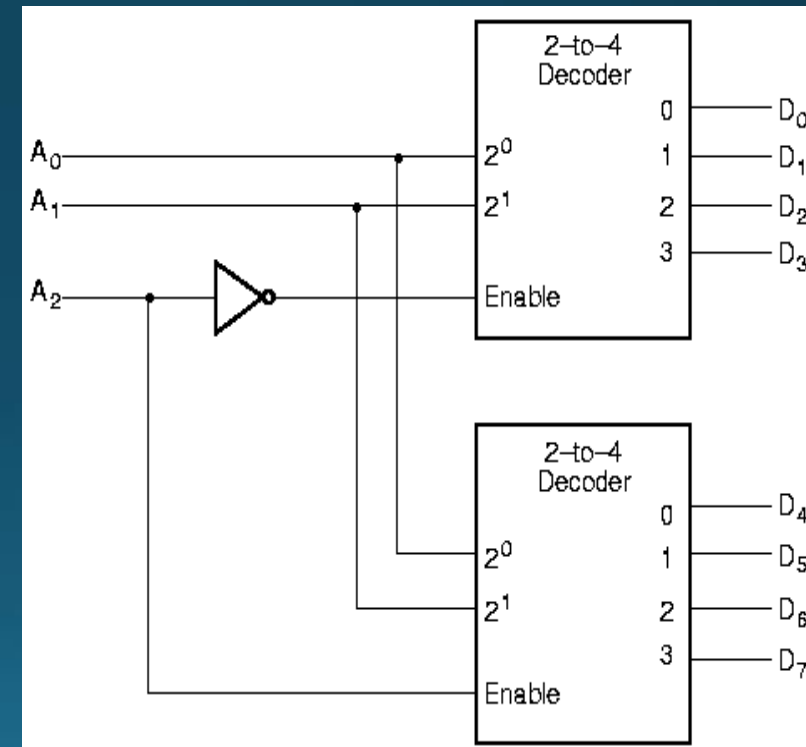
Decoder Expansion



2-4 decoders to form one 3-8 decoder

Combining two 2-4 decoders to form one 3-8 decoder using enable switch

A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0



Encoders

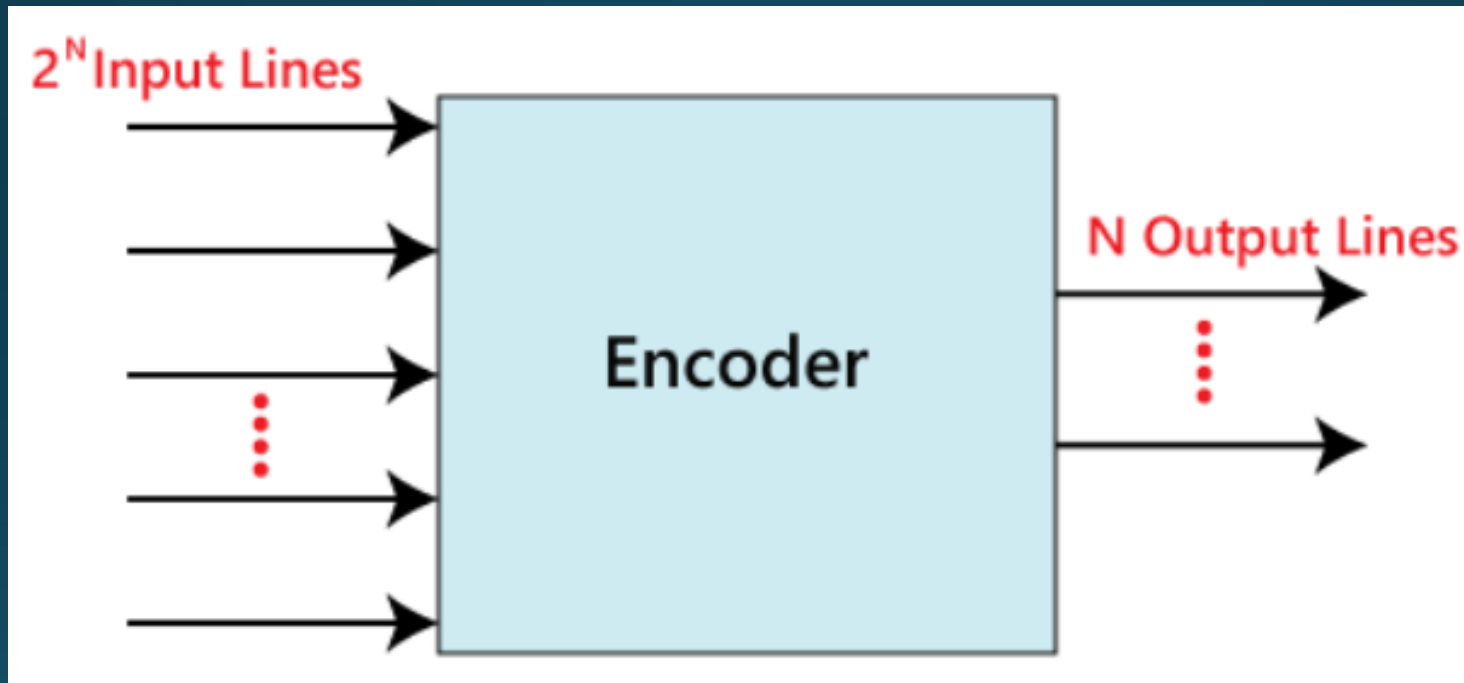
Encoders

- Perform the inverse operation of a decoder
 - ✓ 2^n (or less) input lines and n output lines

Encoders

The combinational circuits that change the binary information into N output lines are known as **Encoders**. The binary information is passed in the form of 2^N input lines. The output lines define the N-bit code for the binary information. In simple words, the **Encoder** performs the reverse operation of the **Decoder**. At a time, only one input line is activated for simplicity. The produced N-bit output code is equivalent to the binary information.

Encoders

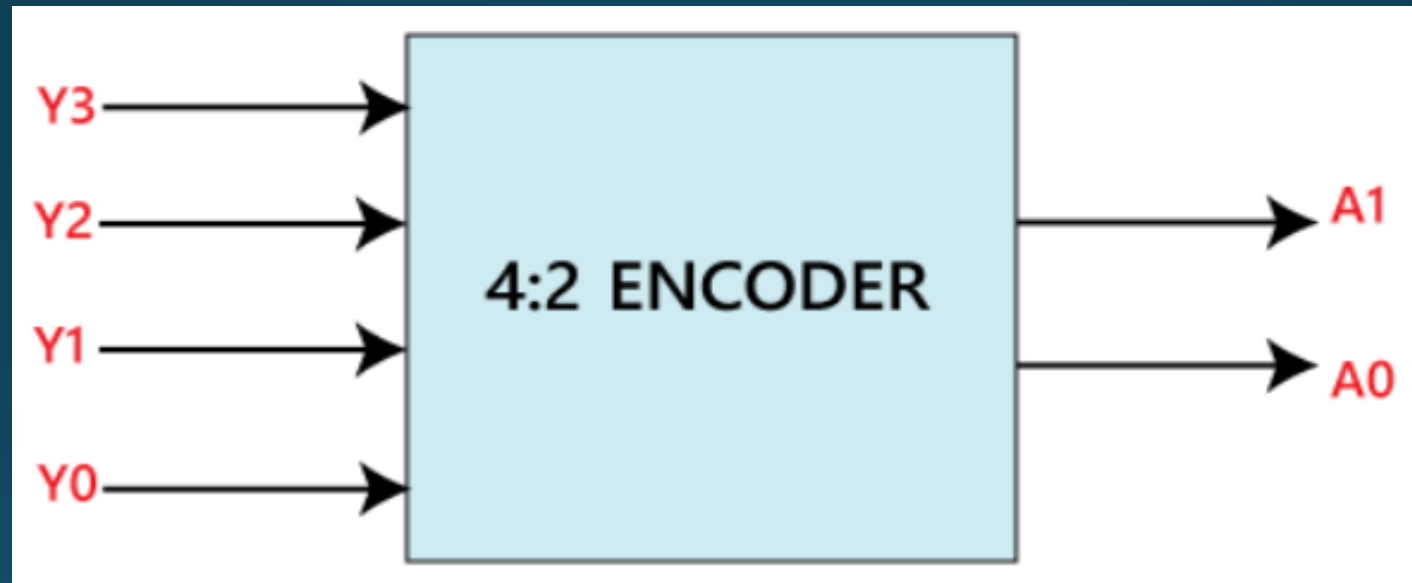


4-to-2 line Encoder

4 to 2 line Encoder

- In 4 to 2 line encoder, there are total of four inputs, i.e., Y_0 , Y_1 , Y_2 , and Y_3 , and two outputs, i.e., A_0 and A_1 . In 4-input lines, one input-line is set to true at a time to get the respective binary code in the output side. Below are the block diagram and the truth table of the 4 to 2 line encoder.

4 to 2 line Encoder



4 to 2 line Encoder

Truth Table:

INPUTS				OUTPUTS	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

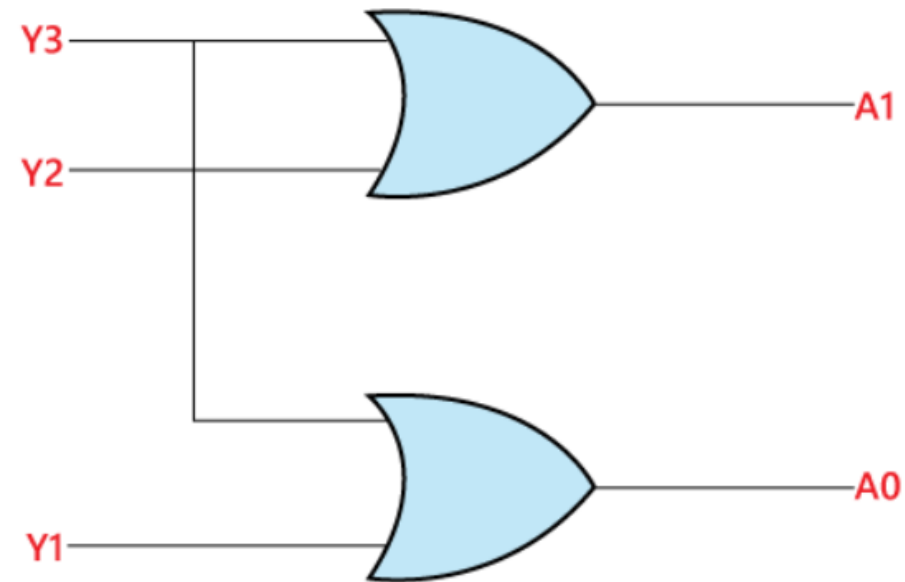
4 to 2 line Encoder

The logical expression of the term A_0 and A_1 is as follows:

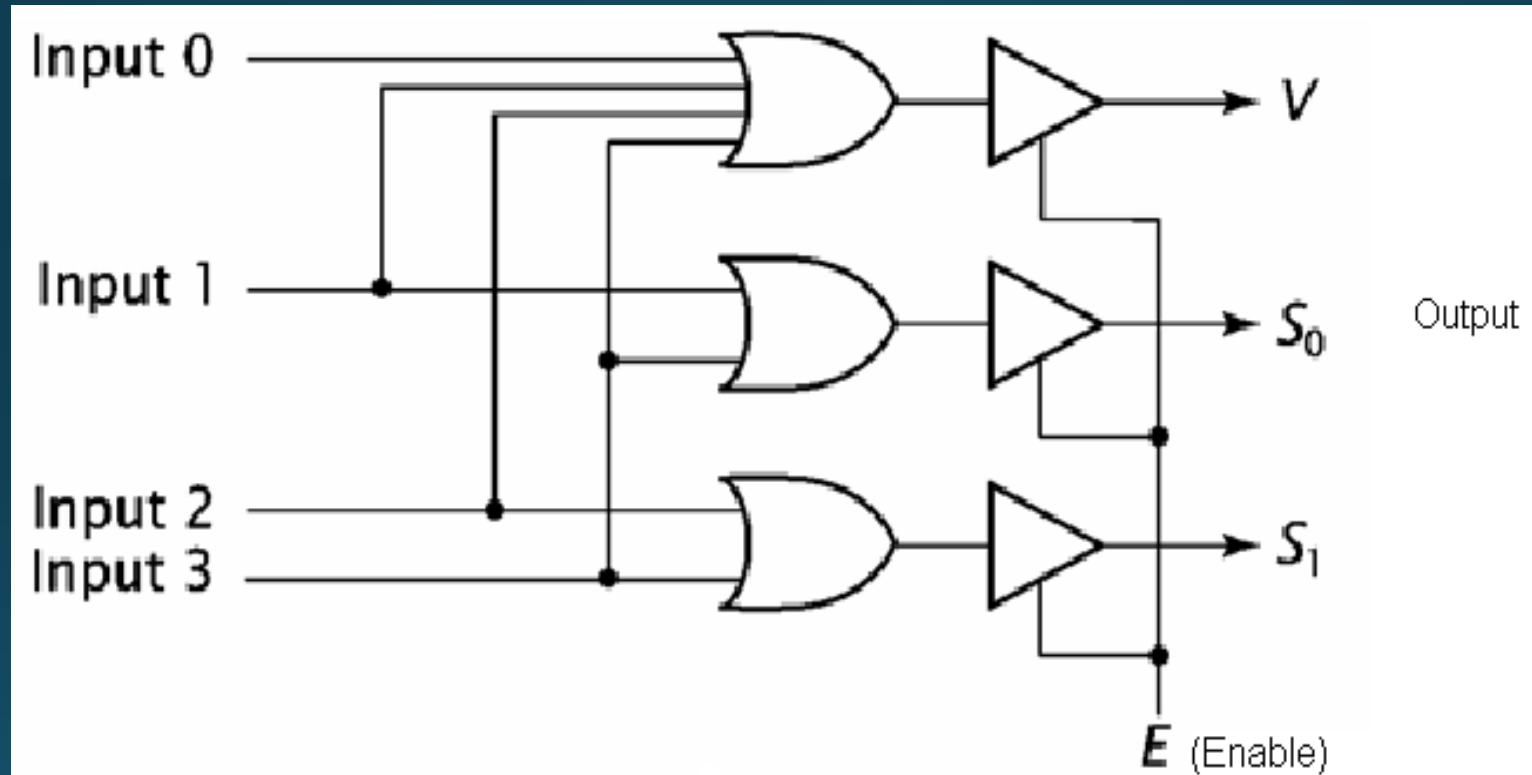
$$A_1 = Y_3 + Y_2$$

$$A_0 = Y_3 + Y_1$$

Logical circuit of the above expressions is given below:



Encoders with OR gates



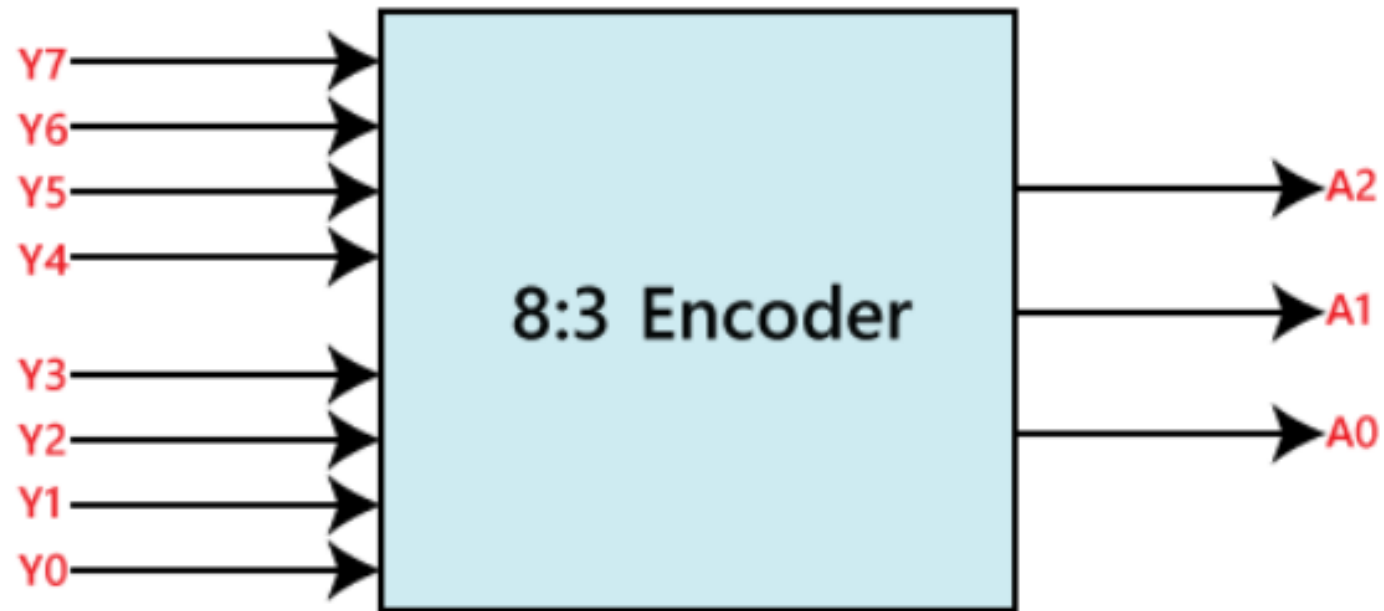
8-to-3 line Encoder

8-to-3 Encoder

The 8 to 3 line Encoder is also known as **Octal to Binary Encoder**. In 8 to 3 line encoder, there is a total of eight inputs, i.e., Y_0 , Y_1 , Y_2 , Y_3 , Y_4 , Y_5 , Y_6 , and Y_7 and three outputs, i.e., A_0 , A_1 , and A_2 . In 8-input lines, one input-line is set to true at a time to get the respective binary code in the output side. Below are the block diagram and the truth table of the 8 to 3 line encoder.

8 x 3 Encoder

Block Diagram:



8 x 3 Encoder

Truth Table:

INPUTS								OUTPUTS		
Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀	A ₂	A ₁	A ₀
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

8 x 3 Encoder

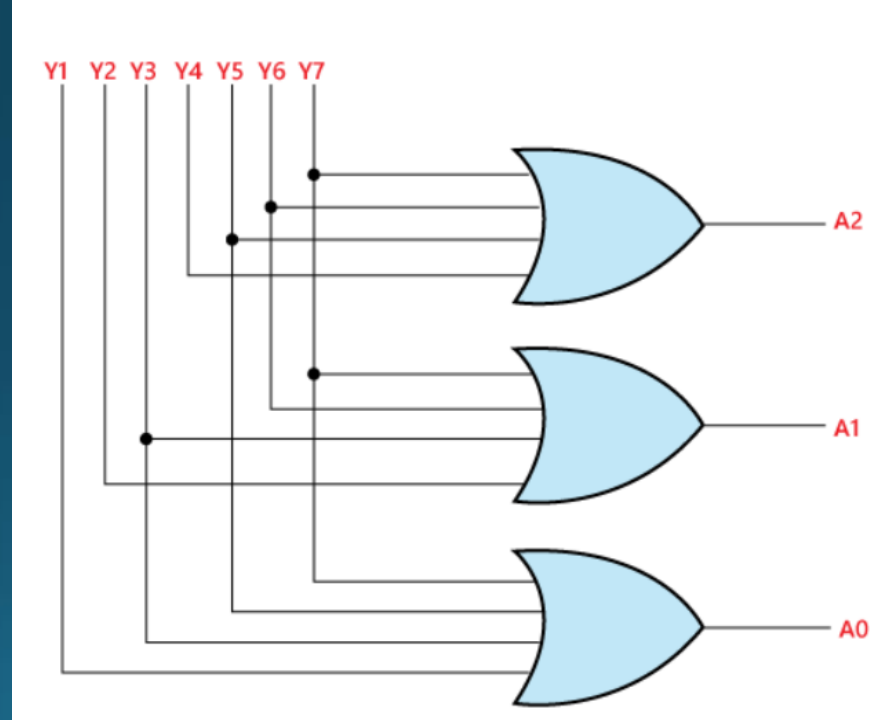
The logical expression of the term A_0 , A_1 , and A_2 are as follows:

$$A_2 = Y_4 + Y_5 + Y_6 + Y_7$$

$$A_1 = Y_2 + Y_3 + Y_6 + Y_7$$

$$A_0 = Y_7 + Y_5 + Y_3 + Y_1$$

Logical circuit of the above expressions is given below:





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